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| 10/723,405 | 11/25/2003 | Frank William Brice JR. | POU920030188US1 | 9082 |

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| EXAMINER | |
|---|---|
| TRUONG, CAMQUY | |

| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/723,405 | BRICE ET AL. | |
| | Examiner | Art Unit | |
| | CAMQUY TRUONG | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/25/03, 3/4/04, 3/27/06, 4/17/06, 5/2/07, 9/10/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-19 are presented for examination.

2. The drawing filed on 12/22/2003 has been acknowledge and acceptable.

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.
Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-19 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-21 of U.S. Patent No. 7,234,037 in view of Shultz (U.S. 4,916,608). Although the conflicting claims are not identical, they are not patentably distinct from each other because both computer systems comprise

substantially the same elements. The differences between claims 1, 18 and 19 of the application and claims 1, 13, 18 and 19 of Patent No. 7,234,037 are allocating at least one of real resource and a virtual resource associated with said first alternate address space to a process.

4. Shultz (U.S. 4,916,608) teaches allocating at least one of a real resource and a virtual resource process (in creating the virtual machine, the control program creates apparent hardware resources consisting of software emulations of processing equipments such as CPU and virtual storage resources, col. 1, lines 35-38; col. 5, lies 22-43) associated with said first alternate address space (col. 8, line 57 – col. 9, line 10).

5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of allocating at least one of a real resource and a virtual resource associated with the first alternate address space as taught by Shultz because this would dynamically providing virtual storage resources to an operating system control program without the need for memory extension. Therefore, it would decrease the overhead cost of the Virtual machine and increase its operation efficiency.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 1-17 are rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The claim language in the following claim is not clearly understood:

i. As to claims 1, 18-19, lines 4-7, it is not clear from the term "in accordance with a definition of a z/Architecture" what applicant is claiming? The definition of the z/Architecture is not defined anywhere in the specification. Applicant must provide more details about what is claimed in the invention.

ii. As to claim 2, line 2, it is not clearly understood whether "an alternate address space" refers to "input output address space" or "first alternate address space" in claim 1; Line 2, it is not clearly indicated whether "an error storage area" refers to " an error storage-area" in line 1, claim 1.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey et al. (U.S. 6,598,144 B1) in view of Shultz (U.S. 4,916,608).

8. As to claim 1, Bailey teaches the invention substantially as claimed including: a method of performing memory mapped input output operations to an alternate address space comprising:

establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data (write operation) in accordance with a definition of a z/Architecture (col. 4, lines 22-65);

establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data ( sending data) in accordance with a definition of a z/Architecture (col. 4, lines 22-65);

ensuring that said selected process corresponds with said process to which said resource is allocated (col. 5, lines 32- 51); and

wherein said process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space (each verbs consumer process 22 requests work to be performed by the host channel adapter, for example, sending data to a destination, or write operation, col. 4, lines 26-29).

9. Bailey does not explicitly teach allocating at least one of a real resource and a virtual resource associated with said first alternate address space to a process. However, Shultz teaches allocating at least one of a real resource and a virtual resource process (in creating the virtual machine, the control program creates apparent hardware resources consisting of software emulations of processing equipments such as CPU

and virtual storage resources, col. 1, lines 35-38; col. 5, lies 22-43) associated with said first alternate address space (col. 8, line 57 – col. 9, line 10).

10. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Bailey by incorporating the teaching of allocating at least one of a real resource and a virtual resource associated with the first alternate address space as taught by Shultz because this would dynamically providing virtual storage resources to an operating system control program without the need for memory extension. Therefore, it would decrease the overhead cost of the Virtual machine and increase its operation efficiency.

11. As to claim 3, Shultz teaches virtualization provides direct access to at least one of a real resource and a virtual resource of an adapter by a problem-state second-level guest process (in creating the virtual machine, the control program creates apparent hardware resources consisting of software emulations of processing equipments such as CPU and virtual storage resources, col. 1, lines 35-38; col. 5, lies 22-43).

12. As to claims 2 and 4, Bailey teaches virtualization of a resource is accomplished and distinguished from a real resource by partitioning a range of resource identifiers into a plurality of portions;

wherein at least one portion corresponds to a virtual resource; and

wherein when at least one of said first instruction and said second instruction specifies a resource identifier corresponding to said at least one portion, the guest issuing said instruction exits, and an underlying host program resumes execution in order to emulate said at least one of said first instruction and said second instruction originally issued by the guest (the addressable range selected may be of different sizes, col. 7, lines 31-60).

13. As to claim 5, Shultz teaches virtualization provides direct access to at least one of a real resource and a virtual resource of an adapter by a problem-state second - level guest process (col. 1, lines 35-38; col. 5, lines 22-43).

14. As to claims 6-7, Shultz teaches access is accomplished without involvement from a kernel of said guest operating system; and permits said process operating in a problem-state maximum efficiency in performing the primary input output capabilities provided by said adapter and the associated resources allocated to said process (col. 5, line 64 – col. 6, line 1).

15. As to claim 8, Bailey teaches said first alternate address space is not a portion of the main address space from which said process is executing (col. 2, lines 28-48).

16. As to claim 9, Bailey teaches said process issuing said at least one of said first instruction and said second instruction and thereby causes execution of at least one of

said store and load with said first alternate address space operates in a problem state of a machine (col. 4, lines 26-31).

17. As to claims 10-11, Bailey teaches problem state corresponds to a least privileged execution state in said z/Architecture (user/kernel, col. 2, lines 10-11).

18. As to claim 12, Bailey teaches at least one of said first instruction and said second instruction is executed without supervisory state intervention (user mode, col. 2, line 11).

19. As to claim 13, Bailey teaches first instruction and said second instruction are semiprivileged instructions that may be executed in problem state, wherein ownership of a specified resource of a specified adapter determines a privilege required for execution of said semiprivileged instructions (user/ kernel mode, col. 2, lines 10-11).

20. As to claims 14-15, Bailey teaches a second alternate address space associated with a second adapter (col. 4, lines 55-65).

21. As to claim 16, Bailey teaches adapter includes address spaces as partitions of said alternate address space (col. 4, lines 60-65).

22. As to claim 17, Bailey teaches an address space is governed by at least one of a

resource type and storage area types associated with an adapter (system and address spaces are for different resources, col. 4, lines 55-65).

23. As to claims 18-19, they are rejected for the same reason as claim 1.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAMQUY TRUONG whose telephone number is (571)272-3773. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai An can be reached on (703)305-9678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

Camquy Truong

September 15, 2008